

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 1 and 2 are currently being amended to clarify those claims. Claims 1-89 are pending in this application, of which claims 12-32, 49 and 53-89 are withdrawn from consideration.

Claim objections

Claims 1 and 2 were objected to for informalities. Claims 1 and 2 have been amended to address the issues raised in the Office Action, and applicants submit that the objections thereto have been overcome.

Rejection under 35 U.S.C. § 112, second paragraph

Claims 1-11, 33-48 and 50-52 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, specifically for language in claims 1 and 2.

In general, claims 1 and 2 have been amended to address the issues raised in the Office Action.

Rejections under 35 U.S.C. §§ 102 and 103

Claims 1-4 and 52 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by U.S. 2002/0036290 to Inaba et al. ("Inaba"). Claims 5-11 and 33-51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba. Applicants respectfully traverse these rejections for at least the following reasons.

Independent claim 1, as amended, recites:

A field effect transistor comprising:
a semiconductor layer projecting upward from the plane of a base and having a lower part and an upper part above the lower part;
a gate electrode provided on both side surfaces of the semiconductor layer;
a gate insulating film interposed between the gate electrode and the said side surfaces of said semiconductor layer; and

source/drain regions where a first conductivity type impurity is introduced in said semiconductor layer,

wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, and has in the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than the concentration of the second conductivity type impurity of the lower part of the semiconductor layer, the second conductivity type impurity being different from the first conductivity type impurity, and

the concentration of the second conductivity type impurity of the channel impurity concentration adjusting region being such that a channel is formed on a side surface portion of the semiconductor layer in the channel impurity concentration adjusting region, which faces said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.

Inaba fails to disclose at least the structure of the above italicized feature of claim 1 in the context of that claim.

As an initial matter, applicants note that the above italicized feature of claim 1 is not merely a process by which the device of claim 1 is made, nor is the feature an intended use of the claim 1 device. Instead the italicized feature of claim 1 provides functional language that defines structure of claim 1 in that it requires “the concentration of the second conductivity type impurity of the channel impurity concentration adjusting region being such that a channel is formed on a side surface portion of the semiconductor layer in the channel impurity concentration adjusting region, which faces said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.”

In contrast to claim 1, Inaba does not disclose “the concentration of the second conductivity type impurity of the channel impurity concentration adjusting region being such that a channel is formed on a side surface portion of the semiconductor layer in the channel impurity concentration adjusting region, which faces said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.” Rather, Inaba discloses that its region 21 in FIG. 7, which the Patent Office equates with the channel impurity concentration adjusting region of claim 1, is for preventing the channel from being formed in the top surface of the substrate projection 11a (See paragraphs [0067], [0068]). Thus, the

impurity concentration of the region 21 in FIG. 7 of Inaba is clearly not such that in a state of operation in which a signal voltage is applied to the gate electrode of Inaba, a channel is located on a side surface portion of the semiconductor layer in the region 21. Thus, Inaba fails to disclose all of the features of claim 1.

Independent claim 2 recites “the concentration of the second conductivity type impurity of the channel impurity concentration adjusting region being such that a channel is formed on upper surface and side surface portions of the semiconductor layer in the channel impurity concentration adjusting region, which face said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode,” and is thus patentable for reasons analogous to claim 1.

The dependent claims under consideration are patentable for at least the same reasons as their respective claims, as well as for further patentable features.

For example, the impurity concentration of claim 4 is more than an intended use, and is not suggested by Inaba.

With respect to the dependent claims rejected as being obvious over Inaba, the Patent Office cites in re Aller, and suggests these claims are merely discovering the optimum or workable range. Applicants respectfully disagree. Inaba provides its region 21 as a means to prevent punch-through (paragraph [0067]. By contrast, embodiments of the invention as claimed provide that a parasitic transistor at the upper corner of the semiconductor layer is inhibited, while at the same time a channel can be formed on the upper portion of the semiconductor layer to reduce channel resistance (See specification, page 28, line 7 to page 29, line 2). Inaba at best suggests optimizing to prevent punch-through, which is quite different from that of the present claims.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorize payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date: March 9, 2009

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